

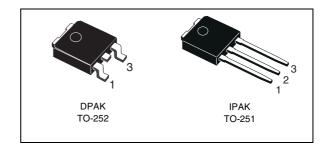
VND10N06 VND10N06-1

"OMNIFET" fully autoprotected Power MOSFET

Features

Max on-state resistance (per ch.)	R _{DS(on)}	0.3Ω
Current limitation (typ)	I _{lim}	10A
Drain-Source clamp voltage	V_{CLAMP}	60V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Logic level input threshold
- ESD protection
- Schmitt trigger on input
- High noise immunity



Description

The VND10N06 and VND10N06-1 are monolithic devices designed in STMicroelectronics VIPower M0-2 technology, intended for replacement of standard Power MOSFETs in DC to 50KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Table 1. Device summary

Package	Order	codes
Fackage	Tube	Tape and reel
DPAK	VND10N06	VND10N06TR
IPAK	VND10N06-1	

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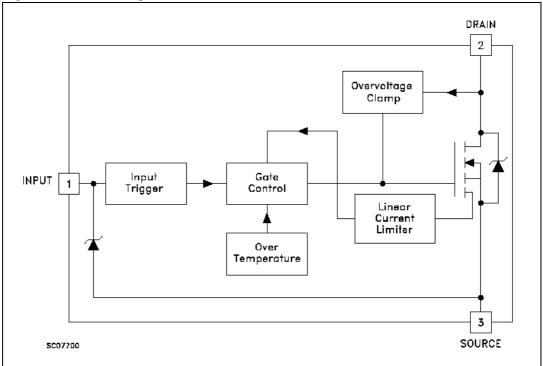
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Block diagram and pin description 1

Figure 1. **Block diagram**



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-Source voltage (V _{in} = 0V)	Internally clamped	V
V _{INn}	Input voltage	Internally clamped	V
I _{in}	Input current	± 20	mA
I _{Dn}	Drain current	Internally limited	Α
I _{Rn}	Reverse DC output current	- 15	Α
V _{ESD}	Electrostatic discharge (R = 1.5KΩ, C = 100pF)	4000	V
P _{tot}	Total dissipation at T _c = 25°C	35	W
T _j	Operating junction temperature	Internally limited	°C
T _c	Case operating temperature	Internally limited	°C
T _{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
R _{thj-case}	Thermal resistance junction-case	3.5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	100	°C/W

2.3 Electrical characteristics

Tcase = 25 °C unless otherwise stated.

Table 4. Off

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{CLAMP}	Drain-Source clamp voltage	V _{IN} = 0V; I _D = 200mA	50	60	70	٧
V _{IL}	Input low level voltage	$I_D = 100 \mu A; V_{DS} = 16 V$			1.5	V
V _{IH}	Input high Level voltage	$R_L = 27\Omega; V_{DD} = 16 V$ $V_{DS} = 0.5 V$	3.2			٧
I _{ISS}	Supply current from input pin	$V_{DS} = 0V; V_{IN} = 5V$		150	300	μΑ
V _{INCL}	Input-Source reverse clamp voltage	$I_{\text{IN}} = -1 \text{mA}$ $I_{\text{IN}} = 1 \text{mA}$	-1 8		-0.3 11	V V
I _{DSS}	Zero input voltage drain current (V _{IN} = 0V)	$V_{DS} = 50V; V_{IN} = V_{IL};$ $V_{DS} < 35V; V_{IN} = V_{IL}$			250 100	μ Α μ Α

Table 5. Switching⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time			1100	1600	ns
t _r	Rise time	$V_{DD} = 16V; I_D = 1A$ $V_{gen} = 7V; R_{gen} = 10\Omega$ (see <i>Figure 2</i>)		550	900	ns
t _{d(off)}	Turn-off delay time			200	400	ns
t _f	Fall time			100	200	ns
t _{d(on)}	Turn-on delay time			1.2	1.8	μs
t _r	Rise time	$V_{DD} = 16V; I_D = 1A$		1	1.5	μs
t _{d(off)}	Turn-off delay time	$V_{gen} = 7V; R_{gen} = 1000\Omega$ (see <i>Figure 2</i>)		1.6	2.3	μs
t _f	Fall time	,		1.2	1.8	μs
(di/dt) _{on}	Turn-on current slope	$V_{DD} = 16V; I_D = 1A$ $V_{in} = 7V; R_{gen} = 10\Omega$		1.5		A/µs
Qi	Total input charge	$V_{DD} = 12V; I_D = 1A; V_{IN} = 7V$		13		nC

^{1.} Parameters guaranteed by design / characterization.

Table 6. On⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
R _{DS(on)}	Static Drain-Source on resistance	$V_{IN} = 7V; I_D = 1 A; T_j < 125 °C$		0.15	0.3	Ω

^{1.} Pulsed: pulse duration = 300μ s, duty cycle 1.5%.

Table 7. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{OSS}	Output capacitance	$V_{DS} = 13V; f = 1MHz; V_{IN} = 0V$		350	500	pF

Table 8. Source Drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	$I_{SD} = 1 A; V_{IN} = V_{IL}$		0.8	1.6	V
t _{rr} ⁽²⁾	Reverse recovery time			125		ns
Q _{rr} ⁽²⁾	Reverse recovery charge	I_{SD} = 1A; di/dt = 100 A/µs V_{DD} = 30V; T_j = 25°C (see <i>Figure 4</i>)		0.22		μC
I _{RRM} ⁽²⁾	Reverse recovery current			3.5		Α

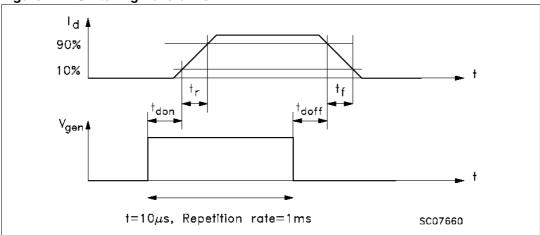
- 1. Pulsed: pulse duration = 300µs, duty cycle 1.5%.
- 2. Parameters guaranteed by design / characterization.

Table 9. Protections (- 40° C < T_i < 150° C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{lim}	Drain current limit	$V_{IN} = 7V; V_{DS} = 13V$	6	10	15	Α
t _{dlim} (1)	Step response current limit	V _{IN} = 7 V; V _{DS} step from 0 to 13V		12	20	μs
T _{jsh} ⁽¹⁾	Overtemperature shutdown		150			°C
T _{jrs} ⁽¹⁾	Overtemperature reset		135			°C
E _{as} (1)	Single pulse avalanche energy	Starting $T_j = 25^{\circ}C$; $V_{DD} = 24V$ $V_{IN} = 7V R_{gen} = 1k\Omega$; $L = 10mH$	250			mJ

^{1.} Parameters guaranteed by design / characterization.

Figure 2. Switching waveforms



R_L 2200 3.3 μF V_{DD} V_{DD} OMNIFET SC07880

Figure 3. Switching time test circuit for resistive load



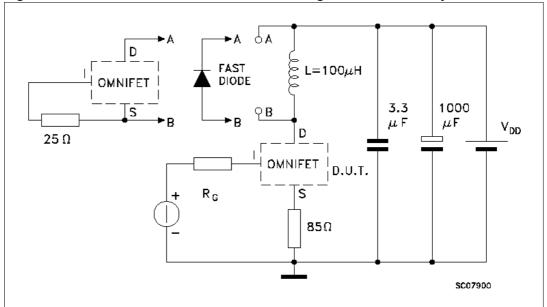
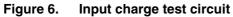
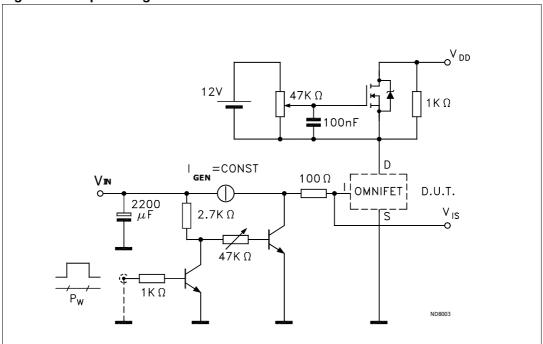


Figure 5. Unclamped inductive load test circuits





V_{DD}
V_{DD}
V_{DD}
V_{DD}
V_{DD}
V_{DD}

Figure 7. Unclamped inductive waveforms

2.4 Electrical characteristics curves

Figure 8. Static Drain-Source on resistance ($V_{\text{IN}} = 3.5V$)

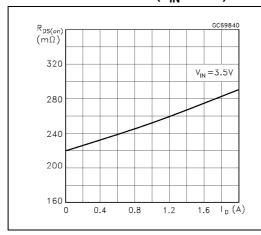


Figure 9. Static Drain-Source on resistance ($V_{IN} = 5V$)

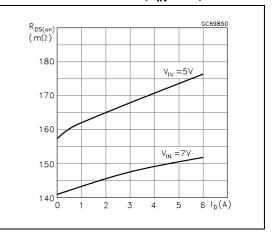
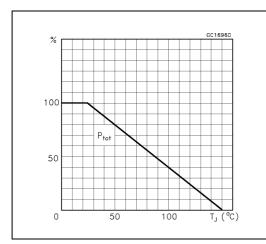


Figure 10. Derating curve

Figure 11. Static Drain-Source on resistance vs. input voltage



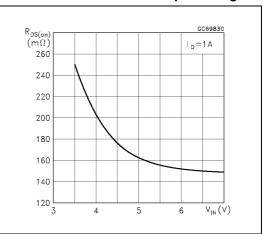
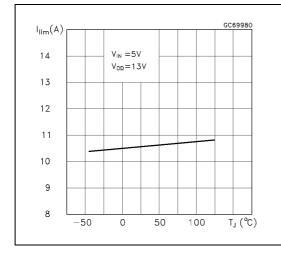


Figure 12. Current limit Vs. junction temperature

Figure 13. Source-Drain diode voltage Vs. junction temperature



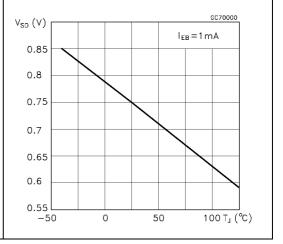
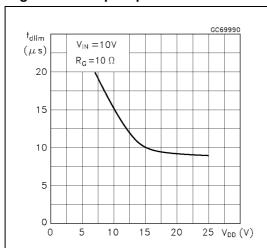


Figure 14. Step response current limit Figure 15. Switching time resistive load



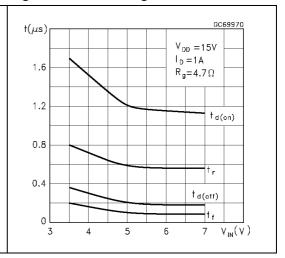
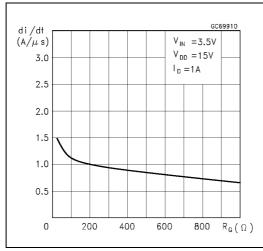


Figure 16. Turn-on current slope $(V_{IN} = 3.5V)$

Figure 17. Turn-on current slope $(V_{IN} = 7V)$



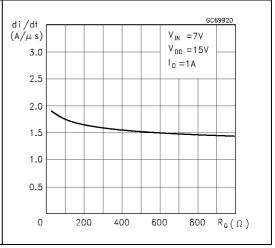
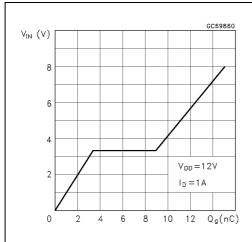
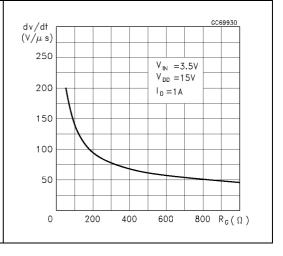


Figure 18. Input voltage Vs. input charge

Figure 19. Turn-off Drain-Source voltage slope





GC69870 GC69940 ${
m dv/dt} \ ({
m V}/{
m \mu \ s})$ C(pF)f = 1 MHz600 250 $V_{IN} = 0V$ $V_{IN} = 7V$ $V_{DD}^{m} = 15V$ 500 200 $I_D = 1A$ 400 150 300 C_{oss} 100 200 50 100 $V_{DS}(V)$ 0 200 400 600 800 $R_{G}(\Omega)$

Figure 20. Turn-off Drain-Source voltage Figure 21. Capacitance variations slope

Figure 22. Switching time resistive load Figure 23. Normalized on resistance Vs. temperature $(V_{IN} = 7V)$

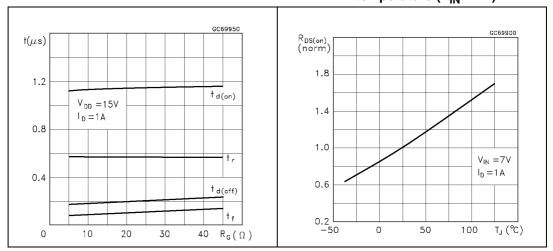
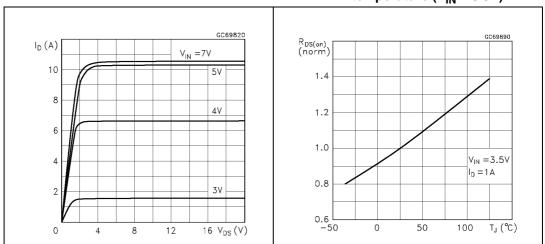


Figure 24. Output characteristics

Figure 25. Normalized on resistance Vs. temperature $(V_{IN} = 3.5V)$



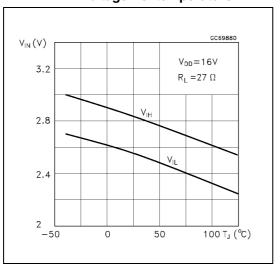


Figure 26. Normalized input threshold voltage Vs. temperature

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3 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path as soon as $V_{IN} > V_{IH}$.

The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50KHz. The only difference from the user's standpoint is that a small DC current $I_{\rm ISS}$ flows into the INPUT pin in order to supply the internal circuitry.

During turn-off of an unclamped inductive load the output voltage is clamped to a safe level by an integrated Zener clamp between DRAIN pin and the gate of the internal Power MOSFET.

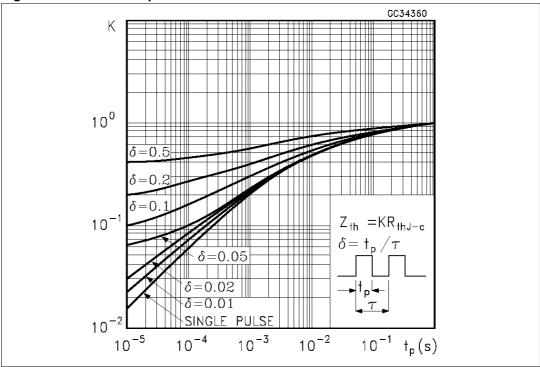
In this condition, the Power MOSFET gate is set to a voltage high enough to sustain the inductive load current even if the INPUT pin is driven to 0V. The device integrates an active current limiter circuit which limits the drain current ID to Ilim whatever the INPUT pin Voltage.

When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the heatsinking capability. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold $T_{\rm ish}$.

If T_j reaches T_{jsh} , the device shuts down whatever the INPUT pin voltage. The device will restart automatically when T_i has cooled down to T_{irs} .

4 Thermal data



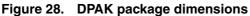


5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 DPAK mechanical data



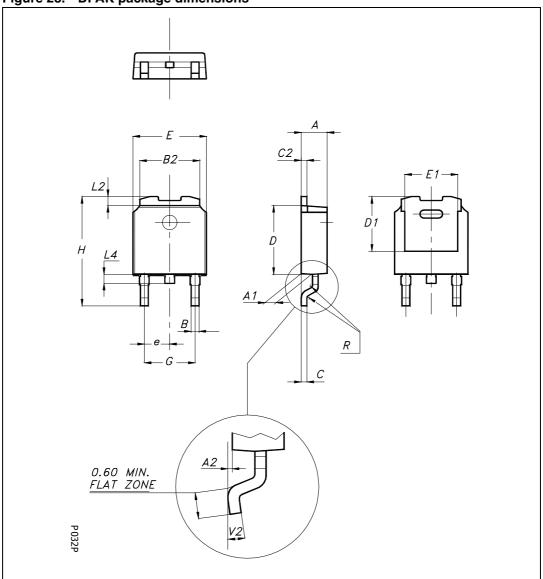


Table 10. DPAK mechanical data

Table 10. DPAK IIIeCI	iailicai uata			
Dim.	Millimeters			
Diiii.	Min.	Тур.	Max.	
A	2.20		2.40	
A1	0.90		1.10	
A2	0.03		0.23	
В	0.64		0.90	
B2	5.20		5.40	
С	0.45		0.60	
C2	0.48		0.60	
D	6.00		6.20	
D1		5.1		
E	6.40		6.60	
E1		4.7		
е		2.28		
G	4.40		4.60	
Н	9.35		10.10	
L2		0.8		
L4	0.60		1.00	
R		0.2		
V2	0°	8°		
Package weight		Gr. 0.29		

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5.3 IPAK mechanical data

Figure 29. IPAK mechanical data and package outline

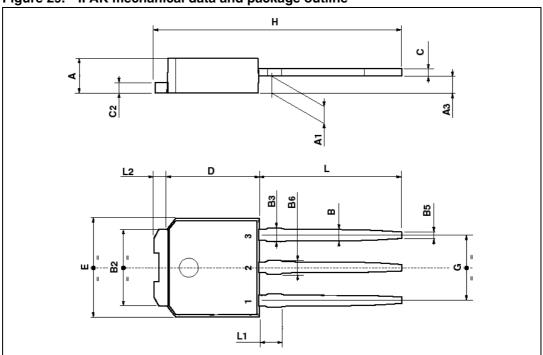


Table 11. IPAK mechanical data

Cumbal	Millimeters				
Symbol	Min.	Тур.	Max.		
A	2.2		2.4		
A1	0.9		1.1		
A3	0.7		1.3		
В	0.64		0.9		
B2	5.2		5.4		
B3			0.85		
B5		0.3			
B6			0.95		
С	0.45		0.6		
C2	0.48		0.6		
D	6		6.2		
E	6.4		6.6		
G	4.4		4.6		
Н	15.9		16.3		
L	9		9.4		
L1	0.8		1.2		
L2		0.8	1		

5.4 DPAK packing information

The devices can be packed in tube or tape and reel shipments (see the *Device summary on page 1*).

Figure 30. DPAK footprint

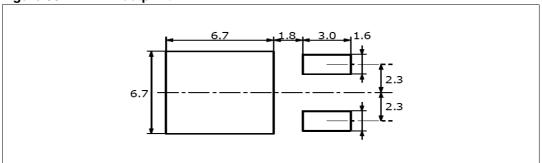
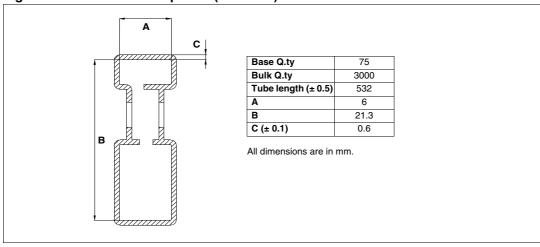


Figure 31. DPAK tube shipment (no suffix)



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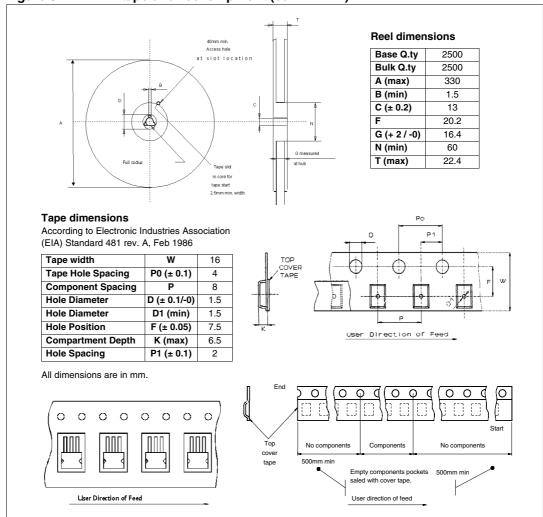
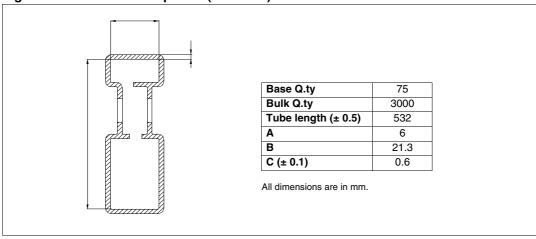


Figure 32. DPAK tape and reel shipment (suffix "TR")

5.5 IPAK packing information

Figure 33. IPAK tube shipment (no suffix)



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6 Revision history

Table 12. Document revision history

Date	Revision	Changes
Oct-1997	1	Initial release.
22-Aug-2006	2	Document restructured.
12-Dec-2008 3		Document restructured and reformatted. Added <i>ECOPACK® packages</i> information.

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